

IN THE CLAIMS

1. (previously presented): A semiconductor device comprising:
 - a base frame including a first surface, and a second surface which opposes said first surface, and including an opening portion formed through the base frame;
 - a semiconductor chip which includes a first main surface on which a plurality of electrode pads is included and a second main surface opposing said first main surface,
 - said semiconductor chip being disposed within said opening portion such that the level of said first main surface is substantially equal to the level of said first surface;
 - an insulating film formed on said first surface and said first main surface such that a part of each of said plurality of electrode pads is exposed;
 - a plurality of wiring patterns which are electrically connected to said plurality of electrode pads, respectively and which extend from said electrode pads to the upper side of the first surface of said base frame, respectively,
 - portions of said wiring patterns on a boundary and vicinity thereof between a region on the upper side of said semiconductor chip and the base frame being wider or thicker than other portions of said wiring patterns;
 - a sealing portion formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and
 - a plurality of external terminals provided included over said wiring patterns in a region including the upper side of said base frame.
2. (original): The semiconductor device according to claim 1, wherein said external terminals are arranged in a region over the upper side of said first surface at a first pitch wider than a second pitch at which said electrode pads are arranged.
3. (original): The semiconductor device according to claim 1, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals, wherein said sealing portion is formed such that a top surface of said electrode posts is exposed.
4. (original): The semiconductor device according to claim 3, wherein said electrode posts are made from a conductive material.

5. (canceled)

6. (original): The semiconductor device according to claim 1, further comprising a lower base for supporting the second main surface of said semiconductor chip and the second surface of said base frame.

7. (original): The semiconductor device according to claim 1, wherein said base frame comprises inside walls which define said opening portion, the thickness of the inside walls gradually decreasing toward said semiconductor chip.

8. (canceled)

9. (withdrawn): The semiconductor device according to claim 1, wherein said base frame comprises a plurality of through holes and an inter-layer wiring which is made from a conductive material and is formed in the holes.

10-17. (canceled)

18. (new): The semiconductor device according to claim 1, wherein said base frame comprises a silicon wafer.

19. (previously presented): A semiconductor device comprising:
a silicon wafer constituting a base frame including a first surface, and a second surface which opposes said first surface, and including an opening portion formed through the base frame;
a semiconductor chip which includes a first main surface on which a plurality of electrode pads is included and a second main surface opposing said first main surface,
said semiconductor chip being disposed within said opening portion such that the level of said first main surface is substantially equal to the level of said first surface;
an insulating film formed on said first surface and said first main surface such that a part of each of said plurality of electrode pads is exposed;

a plurality of wiring patterns which are electrically connected to said plurality of electrode pads, respectively, and which extend from said electrode pads to the upper side of the first surface of said base frame, respectively,

a sealing portion formed on said wiring patterns and said insulating film such that a part of each of said wiring patterns is exposed; and

a plurality of external terminals included over said wiring patterns in a region including the upper side of said base frame.

20. (previously presented): The semiconductor device according to claim 19, wherein said external terminals are arranged in a region over the upper side of said first surface at a first pitch wider than a second pitch at which said electrode pads are arranged.

21. (previously presented): The semiconductor device according to claim 19, further comprising a plurality of electrode posts formed between said wiring patterns and said external terminals,

wherein said sealing portion is formed such that a top surface of said electrode posts is exposed.

22. (previously presented): The semiconductor device according to claim 21, wherein said electrode posts are made from a conductive material.

23. (previously presented): The semiconductor device according to claim 19, further comprising a lower base for supporting the second main surface of said semiconductor chip and the second surface of said base frame.

24. (previously presented): The semiconductor device according to claim 19, wherein said base frame comprises inside walls which define said opening portion, the thickness of the inside walls gradually decreasing toward said semiconductor chip.

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Name _____

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